Precision, 14-bit 8-Channel 600 kSPS SAR ADC

Features

- 14-bit resolution with no missing codes
- Throughput: 600 kSPS
- INL: ±0.2 LSB
- DNL: ±0.15 LSB
- Dynamic Range: 85.5 dB
- SNR: 85 dB
- THD: -103 dB
- Single-ended or Pseudo Differential Range: 0 V ~ V_{REF}
- Pseudo Differential Bipolar Range: ±V_{REF}/2
- No pipeline delay
- Single supply: 2.3 V ~ 5 V
- Logic interface: 1.8 V / 2.5 V / 3 V / 5 V
- Package: QFN-20
- Operating temp range: - 40 °C to +85 °C

Applications

- Relay protection
- Precision data acquisition
- Automated testing
- Battery test
- Optical communication

General Description

The ZJC2102-14 is an 8-channel, 14-bit, SAR analog-to-digital converter (ADC). It operates up to 600 kSPS from a single power supply.

The ZJC2102-14 contains a 14-bit SAR ADC with no missing codes, an 8-channel, low crosstalk multiplexer to configure the inputs as single-ended, pseudo differential unipolar or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and reference driver; a temperature sensor; a selectable one-pole filter; and a digital sequencer which is useful for channels being continuously scanned in order.

The ZJC2102-14 uses a SPI interface for writing configuration register and receiving conversion codes. The digital interface uses a separate supply, VIO, which should be set to the host logic level.

ZJC2102-14 is available in 20-lead QFN packages. It is pin compatible with industry standard parts.

Block Diagram

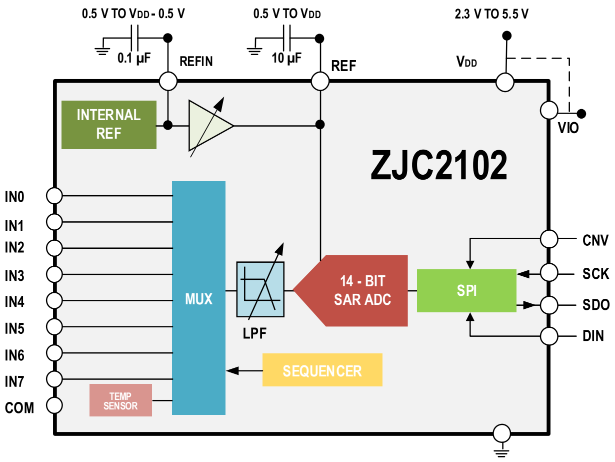

Figure 1. Block Diagram

Typical Characteristics

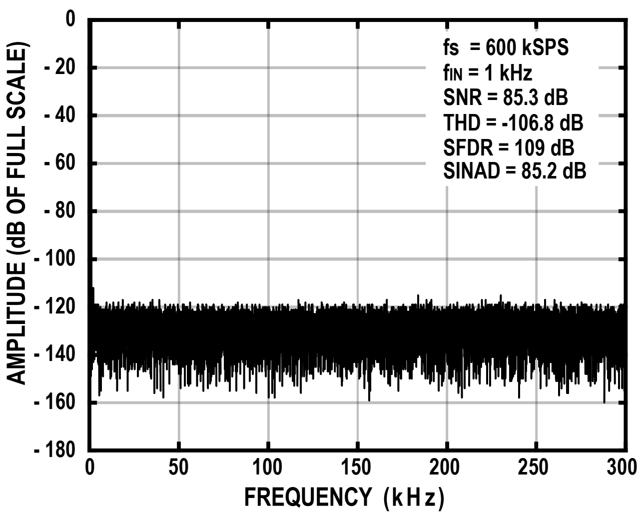

Figure 2. AC Characteristics

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Version (Release B) [1]

Revision History

November 2023 ——Release B

a few pictures and parameters Updated

August 2023 ——Release A

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Pin Configurations and Function Descriptions

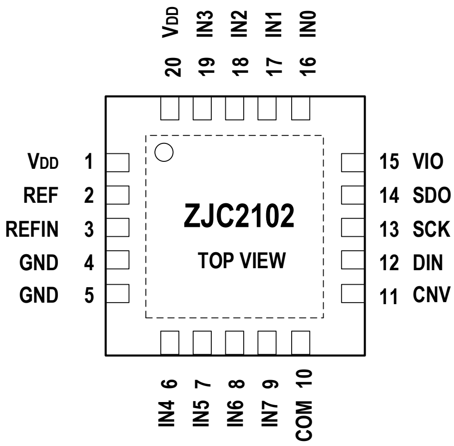


Figure 3. ZJC2102-14 Pin Configuration

Note: The exposed pad has no internal connection. Connect the pad to GND.

Mnemonic	Pin No.	Pin Type	Description
V_{DD}	1, 20	Power Supply	Power Supply. Nominally 2.3 V to 5.5 V when using an external reference and decoupled with 10 μF and 100 nF capacitors. For internal reference 2.5 V output, the minimum V_{DD} should be 3.0 V. For internal reference 4.096 V output, the minimum V_{DD} should be 4.5 V.
REF	2	Analog Input or Output	External Reference Input or Internal Reference Buffer Output. When the internal reference is enabled, it outputs a selectable reference 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered reference voltage of the REFIN pin (4.096 V maximum). This pin needs decoupling with an external 10 μF capacitor close to REF pin. See the Reference Decoupling section.
REFIN	3	Analog Input or Output	Internal Reference Output or External Reference Buffer Input. When using the internal reference, the internal un-buffered bandgap reference voltage is present. It needs decoupling with a 0.1 μF capacitor. When using the internal reference buffer, apply an external reference between 0.5 V and 4.096 V which is buffered to the REF pin.
GND	4, 5	Ground	Power Supply Ground.
IN4	6	Analog Input	ZJC2102-14: Analog Input Channel 4.
IN5	7	Analog Input	ZJC2102-14: Analog Input Channel 5.
IN6	8	Analog Input	ZJC2102-14: Analog Input Channel 6.
IN7	9	Analog Input	ZJC2102-14: Analog Input Channel 7.
COM	10	Analog Input	Common Channel Input. All input channels, IN [7:0], can be referenced to a common-mode point of 0 V or V_{REF}/ 2.
CNV	11	Digital Input	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is high, the busy indictor is enabled.

DIN	12	Digital Input	Serial Data Input. This data input is used for writing to the 14-bit configuration register.
SCK	13	Digital Input	Serial Clock Input. This clock input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
SDO	14	Digital Output	Serial Data Output. The conversion codes are output on this pin by SCK. In unipolar modes, conversion codes are straight binary; in bipolar modes, conversion codes are twos complement.
VIO	15	Digital Power Supply	Digital Interface Power Supply. Nominally at the same supply as the host interface.
IN0	16	Analog Input	ZJC2102-14: Analog Input Channel 0.
IN1	17	Analog Input	ZJC2102-14: Analog Input Channel 1.
IN2	18	Analog Input	ZJC2102-14: Analog Input Channel 2.
IN3	19	Analog Input	ZJC2102-14: Analog Input Channel 3.
EPAD	Exposed Pad	NC	The exposed pad is not connected internally. Recommended connecting the pad to the ground plane.

Absolute Maximum Ratings[1]

Parameter	Rating
V_{DD}, REF, VIO to GND	- 0.3 V ~ 6 V
REF, VIO to V_{DD}	- 6 V ~ V_{DD} + 0.3 V
Analog Input Range (INx to GND)	- 0.3 V ~ V_{DD} + 0.3 V
Digital Input to GND	- 0.3 V ~ VIO + 0.3 V
Digital Output to GND	- 0.3 V ~ VIO + 0.3 V
Storage Temperature Range	- 65 °C to 150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	1.5 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package	$θ_{JA}$	$θ_{JC}$	Unit
QFN-20	51	27	°C/W

1 These ratings apply at 25 °C, unless otherwise noted.
Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
2 IPC/JEDECJ–STD-020 Compliant.
3 Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
4 ANSI/ESDA/JEDEC JS-001 Compliant.
5 ANSI/ESDA/JEDEC JS-002Compliant.
6 $θ_{JA}$ addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted, V_{DD} = 4.5 V ~ 5.5 V, V_{REF} = V_{DD}, T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Resolution				14			
Input Characteristics							
Voltage Range		Unipolar	●	0		V_{REF}	V
		Bipolar	●	- V_{REF}/2		+ V_{REF}/2	
Absolute input voltage		INx+ to GND	●	- 0.1		V_{REF} + 0.1	V
		INx- or COM, Unipolar	●	- 0.1		+0.1	V
		INx- or COM, Bipolar	●	V_{REF}/2- 0.1		V_{REF}/2+0.1	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 230 kHz			67		dB
Leakage Current		Acquisition Phase			1		nA
Input Impedance [1]							
Throughput							
Full Bandwidth		V_{DD} = 4.5 V to 5.5 V	●	0		600	kSPS
		V_{DD} = 2.3 V to 4.5 V	●	0		300	
1/4 Bandwidth		V_{DD} = 4.5 V to 5.5 V	●	0		150	
		V_{DD} = 2.3 V to 4.5 V	●	0		75	
Transient Response		Full - scale step	●			326	ns
DC Accuracy							
No Missing Codes			●	14			bits
Integral Nonlinear Error	INL		●	- 0.75	±0.2	+0.75	LSB [2]
Differential Nonlinear Error	DNL		●	- 0.5	±0.15	+0.5	LSB
Transition Noise		REF = V_{DD} = 5 V			0.3		LSB
Gain Error	GE	Single-ended	●	- 5	±1	+5	LSB
Gain Error Matching					±0.5		LSB
Gain Error Temperature Drift					±0.5		ppm/°C
Zero Error	ZE	Single-ended	●	- 4	±1	+4	LSB
Zero Error Matching					±0.25		LSB
Zero Error Temperature Drift					±0.3		ppm/°C
Power Supply Sensitivity		V_{DD} = 5 V ± 5 %			±0.2		LSB

1 See the Analog Inputs section.
2 LSB means least significant bit. 1 LSB = 305.2 μV for 5 V input range.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
AC Accuracy							
Dynamic Range	DR	V_{REF} = 5 V	●	84.5	85.5		dB[3]
SNR	SNR	f_{IN} = 1 kHz, V_{REF} = 5 V	●	84	85.3		dB
		f_{IN} = 1 kHz, V_{REF} = 4.096 V, internal ref	●	83.5	84.5		
		f_{IN} = 1 kHz, V_{REF} = 2.5 V, internal ref	●	82	83.1		
Signal-to (Noise + Distortion)	SINAD	f_{IN} = 1 kHz, V_{REF} = 5 V	●	84	85.2		dB
		f_{IN} = 1 kHz, V_{REF} = 4.096 V, internal ref	●	83.4	84.4		
		f_{IN} = 1 kHz, V_{REF} = 2.5 V, internal ref	●	82	83		
Spurious-Free Dynamic	SFDR	f_{IN} = 1 kHz, V_{REF} = 5 V			106		dB
Total Harmonic Distortion	THD	f_{IN} = 1 kHz, V_{REF} = 5 V			- 105		dB
Channel Crosstalk		f_{IN} = 1 kHz, V_{REF} = 5 V			- 120		dB
External Reference Input							
Voltage Range		REF Input	●	0.5		V_{DD} + 0.3	V
		REFIN Input (Buffer Enabled)	●	0.5		V_{DD} - 0.5	
Load Current		Sinewave Input			70		μA
Internal Reference Output							
REF Output Voltage		4.096 V, @ 25 °C	●	4.092	4.096	4.100	V
		2.5 V, @ 25 °C	●	2.495	2.5	2.505	
REFIN Output Voltage		REF = 4.096 V, @ 25 °C			2.42		V
		REF = 2.5 V, @ 25 °C			1.21		
REF Output Current					300		μA
Temperature Drift	T_c	- 40 °C to +85 °C	●		6	12	ppm/°C
		0 °C to +85 °C			2		ppm/°C
Line Regulation		V_{DD} = 5 V ± 5 %			20		ppm/V
Turn-On Settling Time		C_{REFIN} = 0.1 μF, C_{REF} = 10 μF			10		ms
Sampling Dynamics							
- 3 dB Analog Input Bandwidth		V_{DD} = 5 V， Full Bandwidth			6		MHz
		V_{DD} = 5 V， 1/4 Bandwidth			1.5		
Aperture Delay		V_{DD} = 5 V			3		ns
Temperature Sensor							
Output Voltage		@ 25 °C			300		mV

[3] Unless otherwise noted, all specifications expressed in decibels (dB) are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full-scale.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Temperature Sensitivity					1		mV/°C
Digital Input							
Logic Level	V_{IL}		•	- 0.3		0.3 x VIO	V
	V_{IH}		•	0.7 x VIO		VIO + 0.3	
Input Current	I_{IL}		•	- 1		+1	µA
	I_{IH}		•	- 1		+1	
Digital Output							
Data Format		Single-ended, or Pseudo Diff Unipolar		Serial 14 -bit, straight binary			
		Pseudo Diff Bipolar		Serial 14 -bit, twos complete			
Logic Low Voltage	V_{OL}	I_{OUT} = +200 µA	•			0.4	V
Logic High Voltage	V_{OH}	I_{OUT} = - 200 µA	•	VIO - 0.3			V
Power Supplies							
V_{DD}		Specified performance		4.5		5.5	V
V_{DD}		Operating Range		2.3		5.5	V
VIO		Specified performance		1.8		V_{DD}+0.3	V
Power-down Current [4,5]		V_{DD} and VIO = 5 V, @25 °C			50		nA
Power Consumption		V_{DD} = 5 V, 1 kSPS	•		32	36	µW
		V_{DD} = 5 V, 100 kSPS	•		3.4	3.8	mW
		V_{DD} = 5 V, 600 kSPS	•		18.6	20.8	mW
		V_{DD} = 5 V, 600 kSPS, internal ref	•		23.3	26.1	mW
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		- 40		+85	°C

4 In the acquisition phase.
5 All digital inputs are forced to VIO or GND as required.

Timing Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise specified, V_{DD} = 4.5 V ~ 5.5 V, V_{REF} = V_{DD}, VIO = 1.8 V ~ V_{DD}, T_A = 25 °C.

Parameter	Symbol		Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	●			1.366	µs
Acquisition Time	t_{ACQ}	●	0.3			µs
Time Between Conversions	t_{CYC}	●	1.666			µs
Data Write/Read During Conversion	t_{DATA}	●			0.8	µs
CNV Pulse Width	t_{CNVH}	●	10			ns
SCK Period (VIO > 3.3 V)	t_{SCK}	●	15			ns
VIO above 2.7 V		●	20			ns
VIO above 2.3 V		●	25			ns
VIO above 1.8 V		●	40			ns
SCK Low Time (VIO > 3.3 V)	t_{SCKL}	●	7.5			ns
SCK High Time (VIO > 3.3 V)	t_{SCKH}	●	7.5			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}					
VIO above 2.7 V		●			17	ns
VIO above 2.3 V		●			18	ns
VIO above 1.8 V		●			21	ns
CNV Low to SDO MSB Valid	t_{EN}					
VIO above 2.7 V		●			22	ns
VIO above 2.3 V		●			25	ns
VIO above 1.8 V		●			28	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}				25	ns
CNV Low to SCK Rising Edge	t_{CLCLK}	●	10			ns
Last SCLK Falling Edge to CNV Rising Edge Delay	t_{QUIET}	●	100			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	●	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	●	5			ns

Timing Specifications Continued

The ● denotes the full temperature range for specified performance. Unless otherwise specified, V_{DD} = 2.3 V ~ 4.5 V, V_{REF} = V_{DD}, VIO = 1.8 V ~ V_{DD}, T_A = 25 °C.

Parameter	Symbol		Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	●			2.633	μs
Acquisition Time	t_{ACQ}	●	2.367			μs
Time Between Conversions	t_{CYC}	●	5			μs
Data Write/Read During Conversion	t_{DATA}	●			0.8	μs
CNV Pulse Width	t_{CNVH}	●	10			ns
SCK Period (VIO > 3.3 V)	t_{SCK}	●	15			ns
VIO above 2.7 V		●	20			ns
VIO above 2.3 V		●	25			ns
VIO above 1.8 V		●	40			ns
SCK Low Time (VIO > 3.3 V)	t_{SCKL}	●	7.5			ns
SCK High Time (VIO > 3.3 V)	t_{SCKH}	●	7.5			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}					
VIO above 2.7 V		●			17	ns
VIO above 2.3 V		●			18	ns
VIO above 1.8 V		●			21	ns
CNV Low to SDO MSB Valid	t_{EN}					
VIO above 2.7 V		●			22	ns
VIO above 2.3 V		●			25	ns
VIO above 1.8 V		●			28	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}				25	ns
CNV Low to SCK Rising Edge	t_{CLCLK}	●	10			ns
Last SCLK Falling Edge to CNV Rising Edge Delay	t_{QUIET}	●	150			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	●	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	●	5			ns

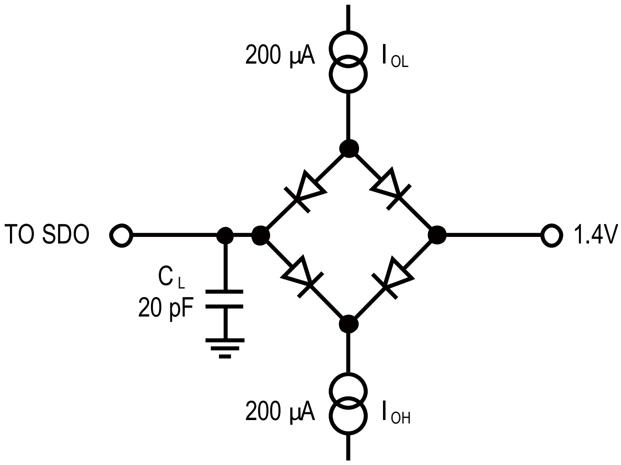


Figure 4. Load Circuit for Digital Interface Timing

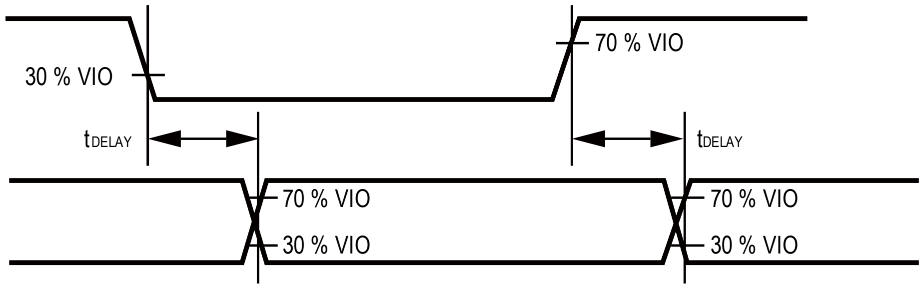


Figure 5. Voltage Levels for Timing

Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, REF = 5.0 V, VIO = 3.3 V, T_A = 25 °C.

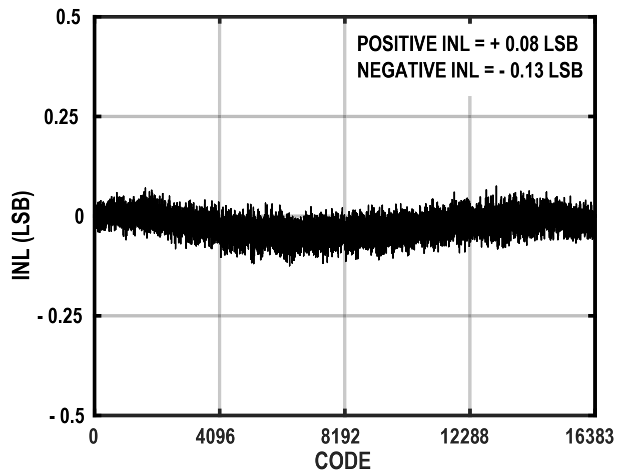


Figure 6. Integral Nonlinearity vs. Code

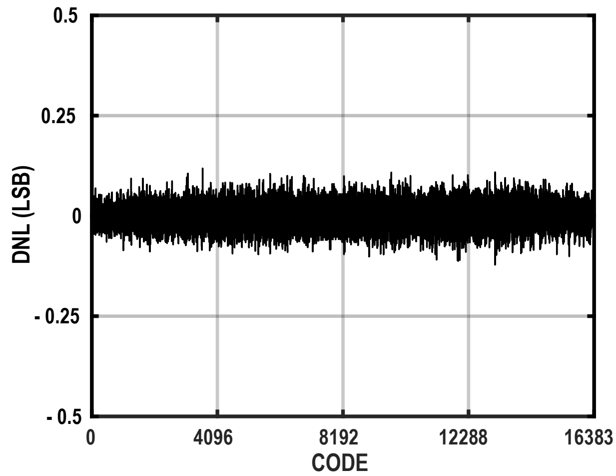


Figure 7. Differential Nonlinearity vs. Code

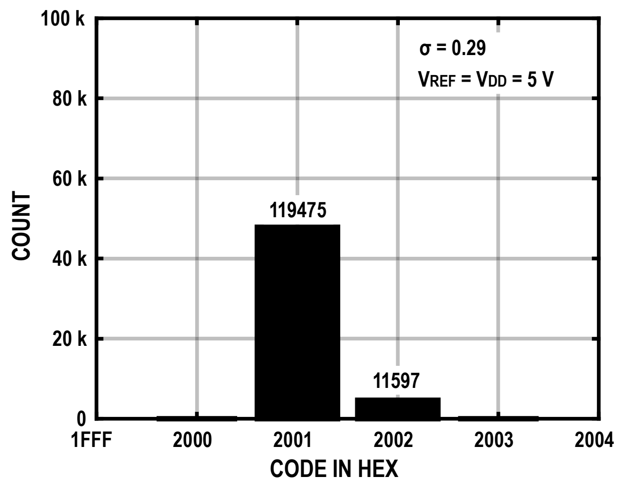


Figure 8. Histogram of DC Input (Code Center)

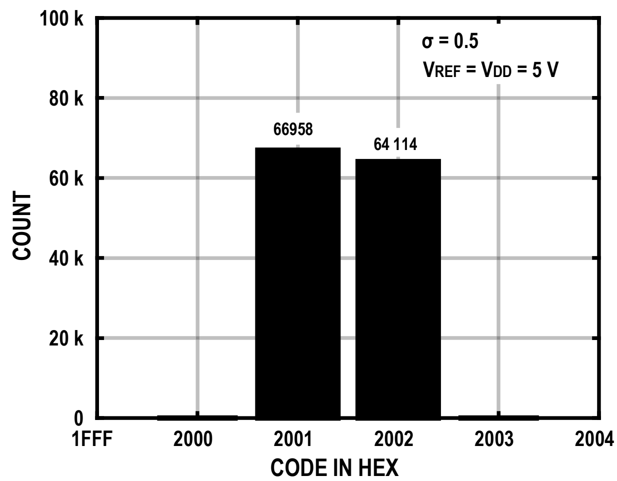


Figure 9. Histogram of DC Input (Code Transition)

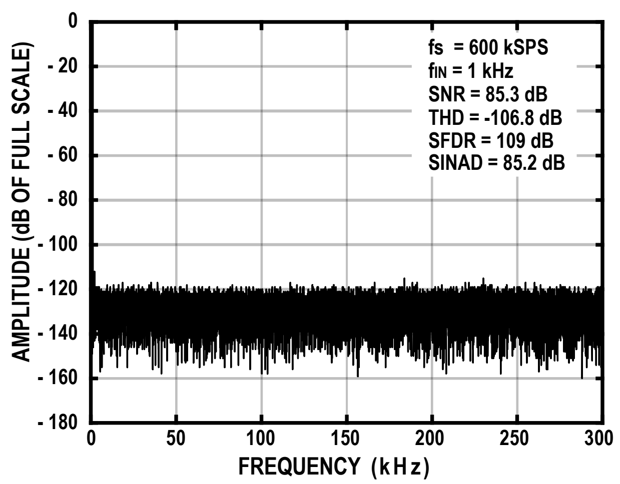


Figure 10. FFT Plot V_{REF} = V_{DD} = 5 V

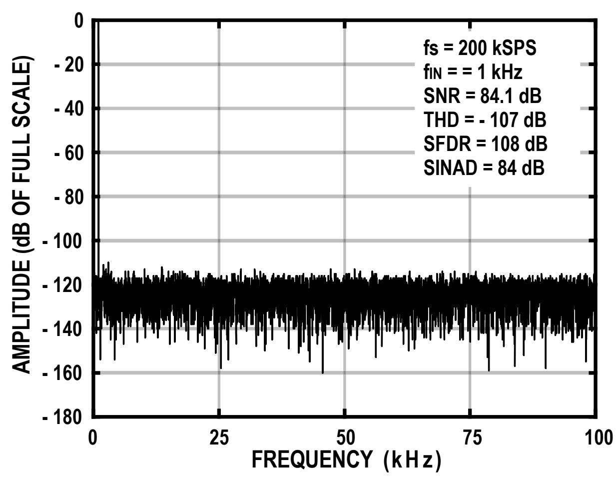


Figure 11. FFT Plot V_{REF} = V_{DD} = 2.5 V

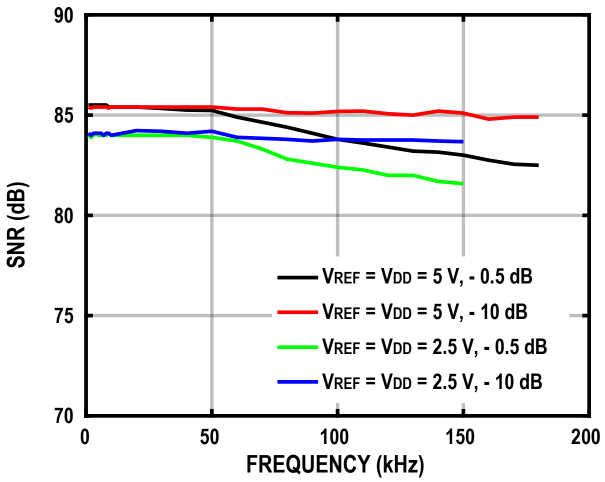


Figure 12. SNR vs Frequency

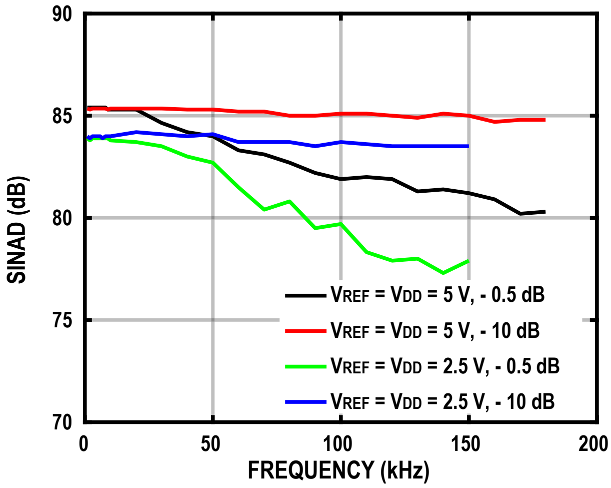


Figure 13. SINAD vs Frequency

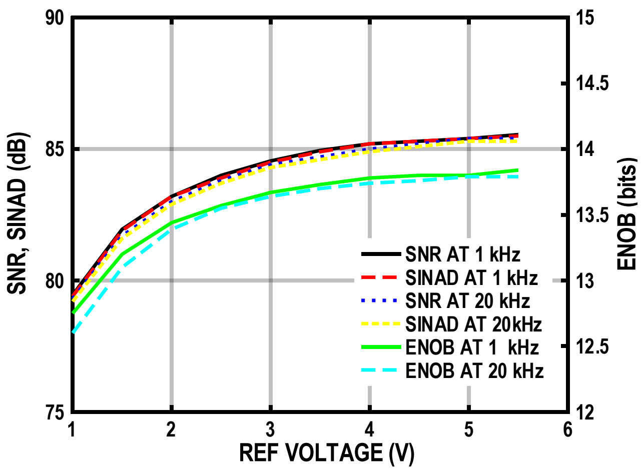


Figure 14. SNR, SINAD and ENOB vs. Reference Voltage

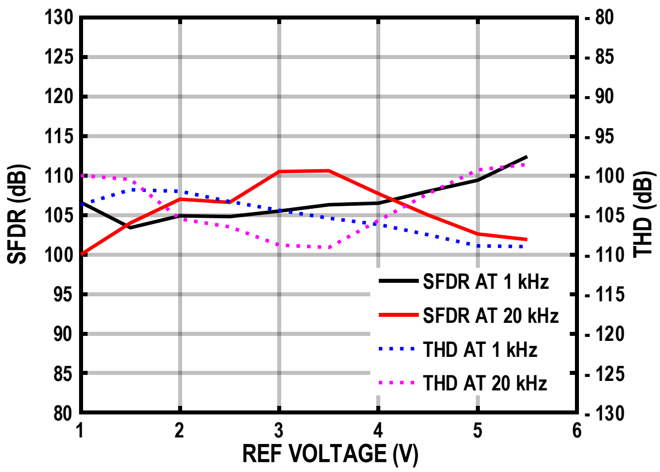


Figure 15. THD, SFDR vs. Reference Voltage

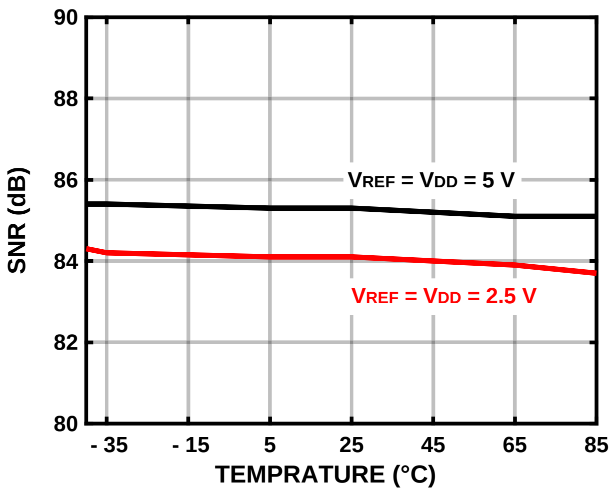


Figure 16. SNR vs. Temperature

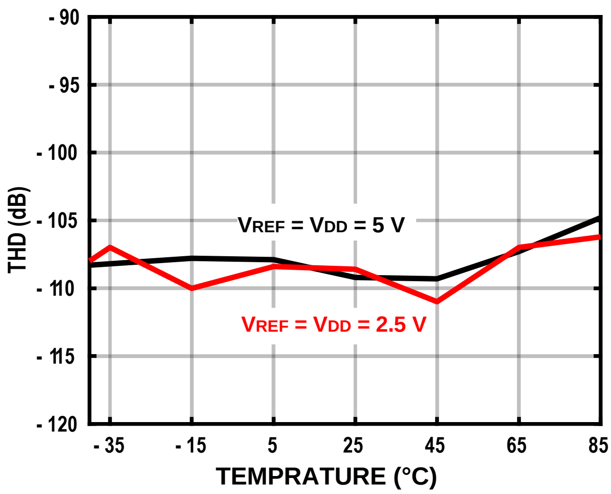


Figure 17. THD vs. Temperature

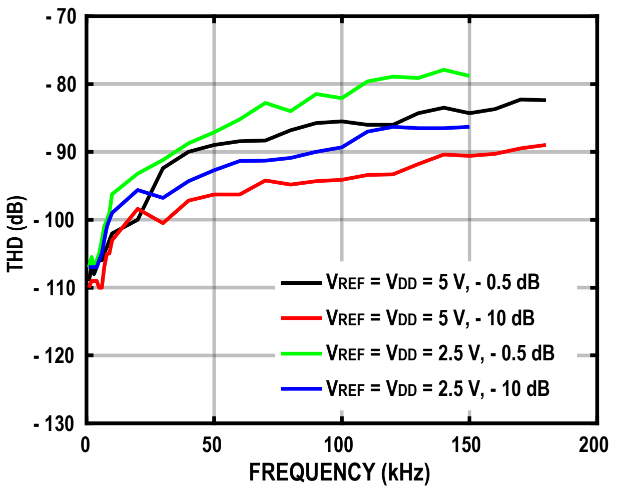


Figure 18. THD vs. Frequency

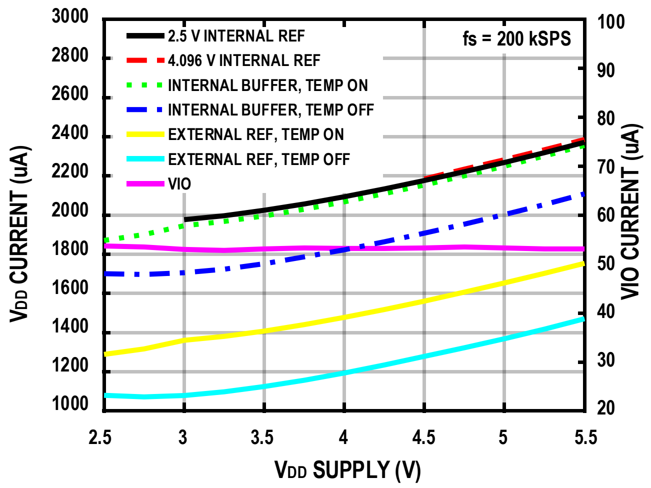


Figure 19. VDD and VIO Current vs. VDD Supply

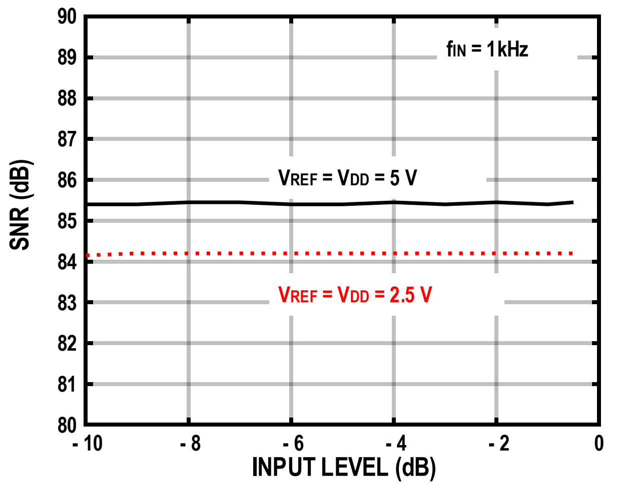


Figure 20. SNR vs. Input Voltage

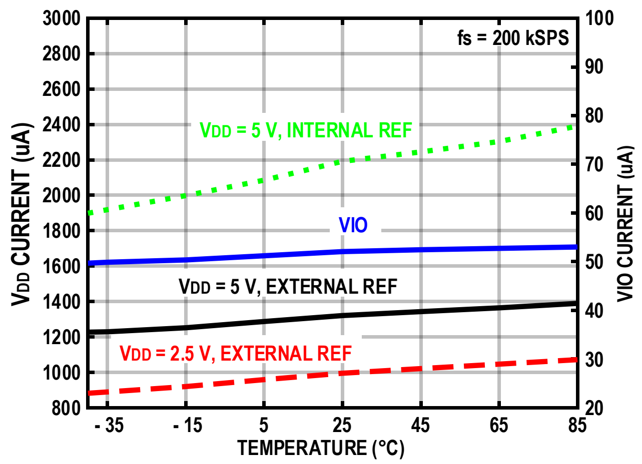


Figure 21. VDD and VIO Current vs. Temperature

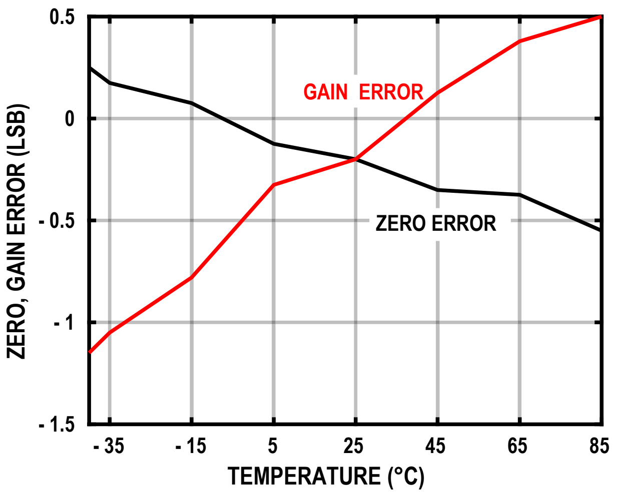


Figure 22. Zero Input, Gain Error vs. Temperature

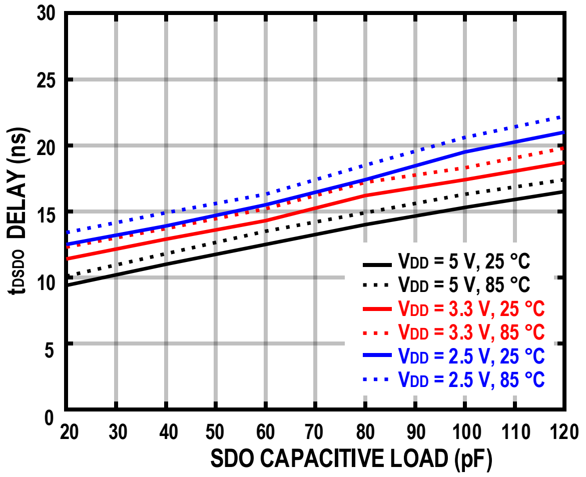


Figure 23. tDSDO Delay vs Capacity Load and Voltage

Theory of Operation

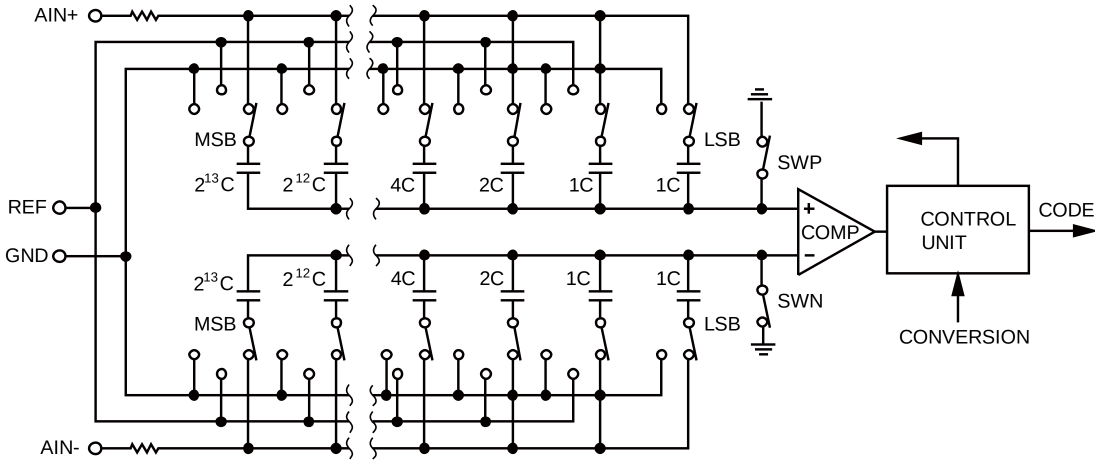


Figure 24. ADC Simplified Circuit Diagram

Circuit Structure

The ZJC2102-14 is an 8-channel, 14-bit, charge redistribution successive approximation register analog-to-digital converter. The ZJC2102-14 is capable of running up to 600 kSPS and powers down between conversions.

The ZJC2102-14 contains a 14-bit SAR ADC, an 8-channel, low crosstalk multiplexer to configure the inputs as single-ended, pseudo differential unipolar or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and reference driver; a temperature sensor; a selectable one-pole filter; and a digital sequencer which is useful for channels being continuously scanned in order.

Convertor Operation

Figure 24 is a simplified circuit diagram of ZJC2102-14.

In the acquisition phase, the array node connected to the input of the comparator is short connect to GND via the SW+ and SW-. All individual switches are connected to analog inputs. When the acquisition phase is complete and a rising edge occurs on the CNV input, the conversion phase is initiated. When the conversion phase begins, the SW+ and SW-disconnect first. The two capacitor arrays are then disconnected from the input and connected to the GND input. By switching the elements of the capacitor array between GND and REF, the comparator input will vary in binary weighted voltage steps ($V_{REF}/2^1$, $V_{REF}/2^2$, ..., $V_{REF}/2^{13}$). The control logic toggles these switches in sequence starting with the MSB, and the comparator is brought back into balance each time. After this phase is complete, the device returns to the acquisition phase, and the control logic generates the ADC output code.

Transfer Function

When configured as singled-ended or pseudo differential unipolar (single-ended INx to GND, COM to GND, temperature sensor, IN- to GND), the code is straight binary. The ideal transfer characteristic is shown below:

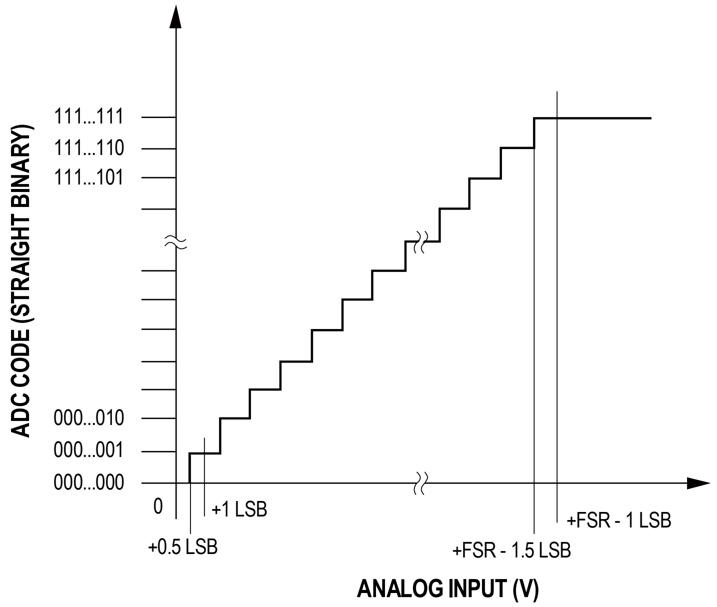


Figure 25. ADC Ideal Transfer Function of Singled-ended or Pseudo Differential Unipolar

Singled-ended or Pseudo Differential Unipolar Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR - 1 LSB	4.999695 V	0x3FFF [1]
Midscale + 1 LSB	2.500305 V	0x2001
Midscale	2.5 V	0x2000
Midscale - 1 LSB	2.499695 V	0x1FFF
- FSR + 1 LSB	305.2 µV	0x0001
- FSR	0 V	0x0000 [2]

When configured as pseudo differential bipolar (COM = V_{REF}/2 or INx- = V_{REF}/2), the code is twos complement.

1 This is also the code for an overranged analog input ((INx+) − (INx−), or COM, above V_{REF} − GND).
2 This is also the code for an underranged analog input ((INx+) − (INx−), or COM, below GND).

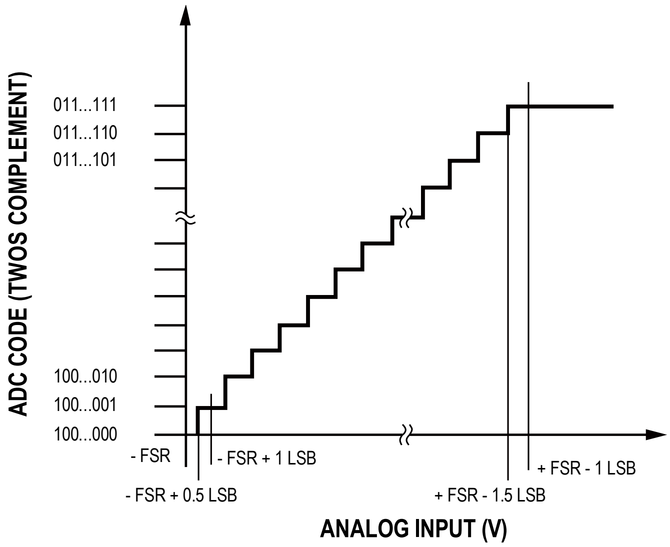


Figure 26. ADC Ideal Transfer Function of Pseudo Differential Bipolar

Pseudo Differential Bipolar Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR - 1 LSB	+2.499695 V	0b01 1111 1111 1111 [1]
Midscale + 1 LSB	+305.2 µV	0b00 0000 0000 0001
Midscale	0 V	0b00 0000 0000 0000
Midscale - 1 LSB	- 305.2 µV	0b11 1111 1111 1111
- FSR + 1 LSB	- 2.499695 V	0b10 0000 0000 0001
- FSR	- 2.5 V	0b10 0000 0000 0000 [2]

1 This is also the code for an overranged analog input ((INx+) − (INx−), or COM, above V_{REF} − GND).
2 This is also the code for an underranged analog input ((INx+) − (INx−), or COM, below GND).

Typical Connection

Figure 27 is a suggested connection for the ZJC2102-14 when multiple power supplies are used.

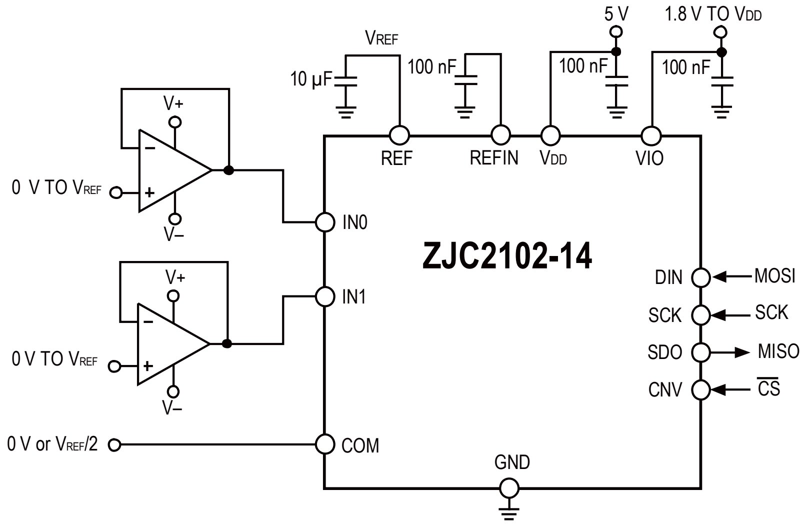


Figure 27. Application Circuits Using Multiple Power Supplies

Figure 28 shows the equivalent circuit of the ZJC2102-14 input structure.

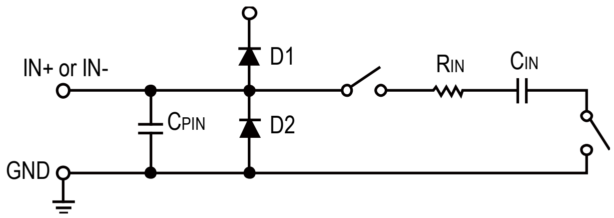


Figure 28. Two Diodes D1 and D2 Provide ESD Protection for the Analog Inputs

The voltage of the analog input signal cannot be higher than the supply voltage (V_{DD}) by more than 0.3 V. If the voltage of the analog input signal exceeds V_{DD} + 0.3 V, the diode will be forward biased and start conducting current. These two diodes can handle forward bias currents up to 50 mA. If the supply voltage of the input driver is higher than V_{DD} the voltage of the analog input signal may be more than 0.3 V higher than the supply voltage. The two diodes D1 and D2 provide ESD protection for analog input IN+ and IN-.

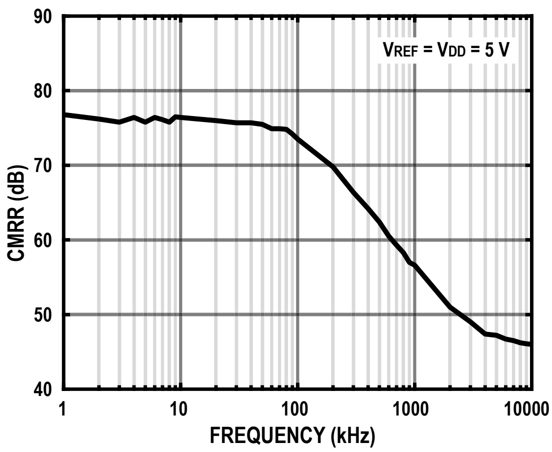


Figure 29. Analog Input CMRR vs. Frequency

In the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 700 Ωand is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

Fully Differential to Single-ended Driver

For applications using fully differential analog signals (bipolar or unipolar), an op amp driver can provide pseudo differential unipolar input to the ZJC2102-14, see Figure 30 for the schematic diagram.

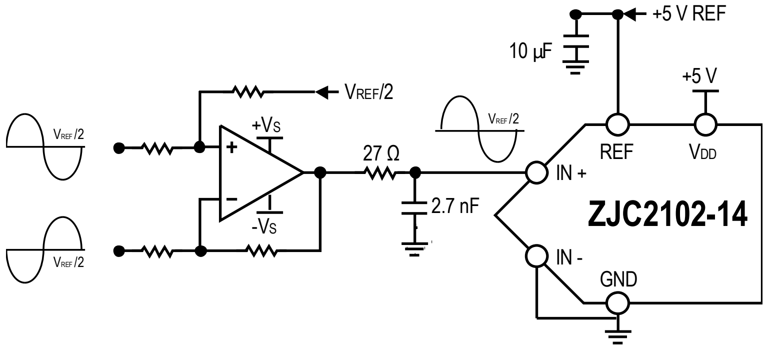


Figure 30. Fully Differential to Single-ended Conversion with an Op Amp

Singled-ended bipolar signal can be converted to pseudo differential unipolar signal with two amplifiers for ZJC2102-14.

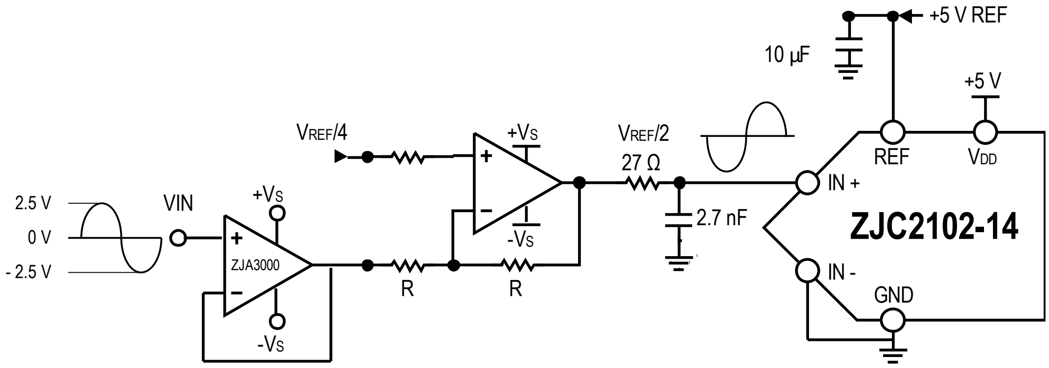


Figure 31. Single-ended Bipolar to Pseudo Differential Unipolar

Input Configurations

Figure 32 shows configuring the analog inputs with the configuration register CFG [12:10].

The analog inputs can be configured as:

- Figure 32A, all single-ended INx inputs referenced to ground; CFG [12:10] = 111. In this configuration, all inputs (IN [7:0]) have a range of GND to V_{REF}.
- Figure 32B, pseudo differential bipolar with a common reference point; COM = $V_{REF}/2$; CFG [12:10] = 010. Pseudo differential unipolar with COM = 0 V; CFG [12:10] = 110. All inputs IN [7:0] referred to GND have a range of GND to V_{REF}.
- Figure 32C, pseudo differential bipolar pairs with the negative input channel referenced to $V_{REF}/2$; CFG [12:10] = 00X.Pseudo differential unipolar pairs with the negative input channel referenced to a ground sense; CFG [12:10] = 10X. In these configurations, the positive input channels have the range of GND to V_{REF}. The negative input channels are senses referred to $V_{REF}/2$ for bipolar pairs, or GND for unipolar pairs. If CFG [9:7] is even, then IN0, IN2, IN4, and IN6 are used as positive inputs. If CFG [9:7] is odd, then IN1, IN3, IN5, and IN7 are used as positive inputs. Note that for the sequencer, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 32D, inputs configured in any of the combinations above.

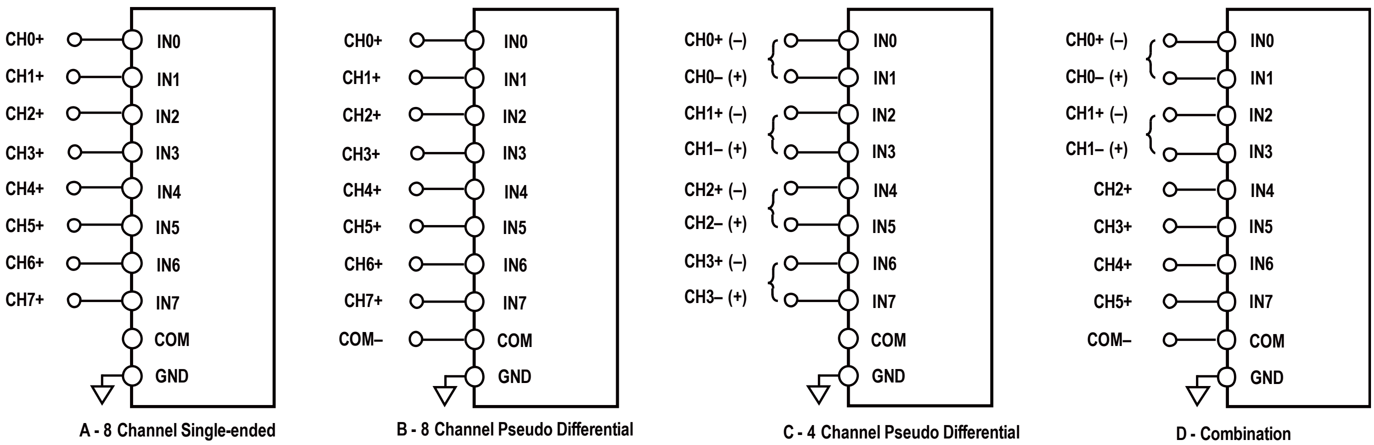


Figure 32. Multiplexed Analog Input Configurations

Internal Reference / Temperature

The ZJC2102-14 internal precision reference, can be set for either a 2.5 V or a 4.096 V on REF pin. When the internal reference is enabled, the band gap voltage is present on the REFIN pin. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the ZJA3000. Note that the voltage of REFIN changes depending on the 2.5 V or 4.096 V internal reference.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the ZJC2102-14. Note that, when using the temperature sensor, the output is straight binary referenced ZJC2102-14 GND pin.

The internal reference is trimmed to provide a typical drift of ±6 ppm/°C. Figure 33 shows the internal reference connection.

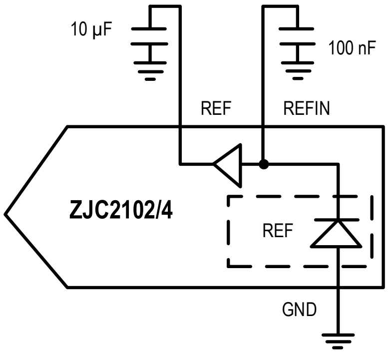


Figure 33. 2.5 V or 4.096 V Internal Reference Connection

External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 34. The external source is connected to REFIN, the input to the on-chip unity gain buffer, and the output is produced on the REF pin to drive the ADC core. An external reference can be used with the internal buffer with or without the temperature sensor enabled.

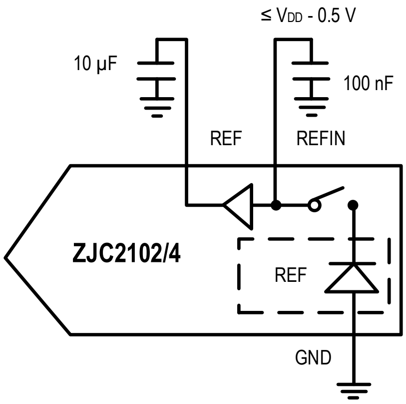


Figure 34. External Reference Using Internal Buffer

External Reference

For improved drift or noise performance, an external reference can be connected directly on the REF pin as shown in Figure 34.The reference buffer must be powered down, and the internal reference can be disabled for lower power consumption.

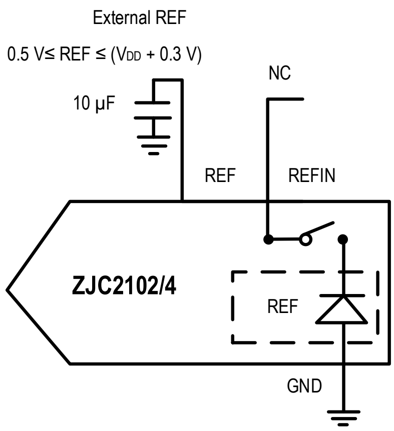


Figure 35. External Reference (internal buffer disabled)

For precision ADC applications, a precision voltage reference is an essential device. Generally, the reference source needs to have low initial error, low noise, and low temperature drift. The ZJC2102-14 reference voltage REF has a dynamic input impedance, so it should be driven with a low impedance source. The REF and GND pins should be effectively decoupled as described in the PCB Layout Guidelines section. Figure 36 shows an example of a specific voltage reference and driver design. The ZJR100X series of high-precision voltage references can just meet these requirements.

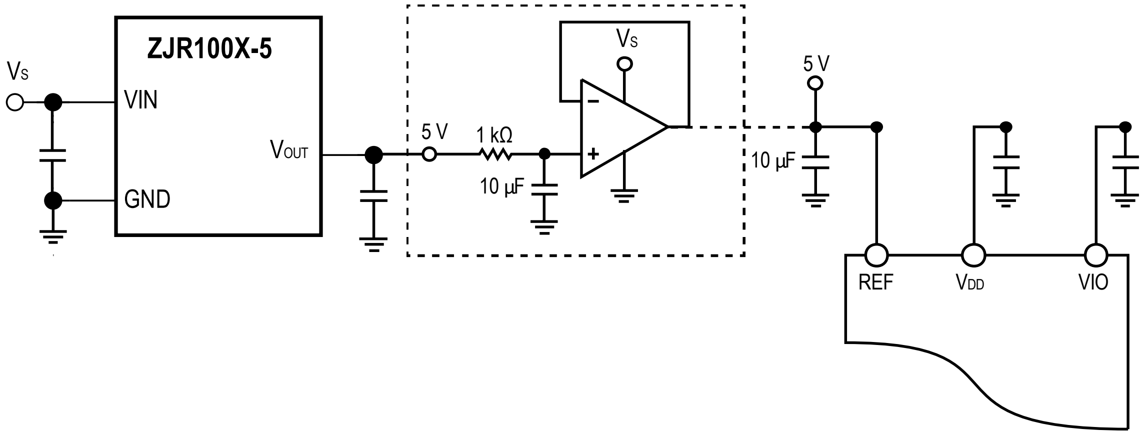


Figure 36. External Reference Drive

Power Supply

ZJC2102-14 uses two power supply pins: core power supply (V_{DD}) and digital input/output interface power supply VIO. VIO can directly interface with any logic from 1.8 V to V_{DD}. To reduce the number of power supplies required, the VIO and V_{DD} pins can be tied together via resistors or ferrite beads. The PSRR curve is shown in Figure 37.

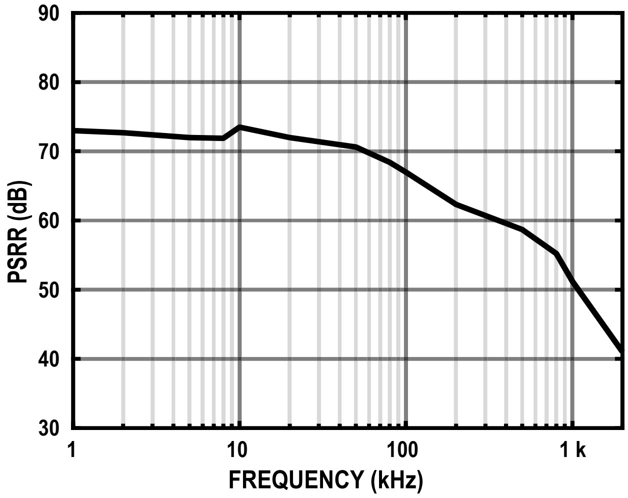


Figure 37. PSRR vs. Frequency

The ZJC2102-14 automatically enters power-down mode at the end of each conversion stage, so the power consumption is approximately linearly proportional to the sampling rate. This makes the device suitable for low sampling rate and low power consumption applications. As shown Figure 38.

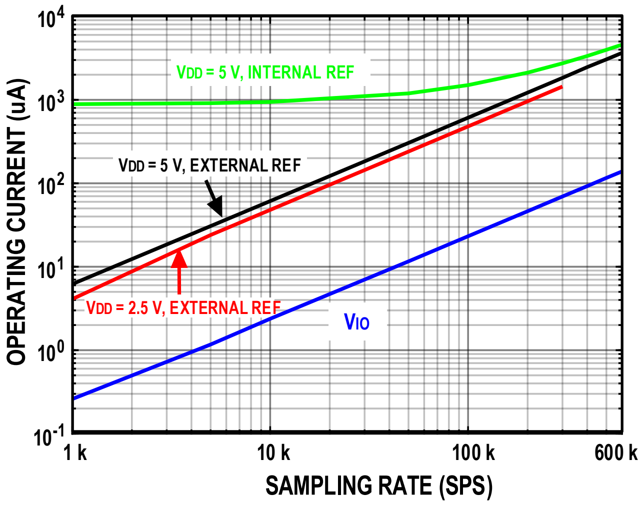


Figure 38. Operating Current vs. Sampling Rate

Digital Interface

ZJC2102-14 has 4-wire SPI digital interface which uses CNV, DIN, SCK and SDO. A 14-bit register, CFG [13:0], is used to configure the ADC for the channel to be converted, the reference selection, and other components.

When CNV is low (works like chip select), reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion), as detailed in the following sections. The CFG word is updated on the first 14 SCK rising edges, and conversion codes are output on the first 13 (or 14 if busy indicator is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word following the conversion code with the CFG MSB following the LSB of the conversion code.

Reading / Writing During Conversion

When reading or writing during conversion (n), conversion results are for the previous (n - 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion. After the CNV is brought high to initiate conversion, it must be brought low again to allow reading or writing during conversion. Reading or writing should only occur up to t_{DATA}.

The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA}}$$

The time between t_{DATA} and t_{CONV} is a quiet time when digital activity should not occur, or sensitive bit decisions may be corrupted.

Reading / Writing After Conversion

When reading or writing after conversion, or during acquisition (n), conversion results are for the previous (n - 1) conversion, and writing is for the (n + 1) acquisition. The reading or writing takes place during the t_{ACQ} (minimum) time.

Reading / Writing Spanning Conversion

When reading or writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n - 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Configuration Register

The ZJC2102-14 uses a 14-bit configuration register (CFG [13:0]) to configure the analog inputs, the channel to be converted, the one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges.

The register can be written to during conversion, during acquisition, or spanning acquisition/conversion, and is updated at the end of conversion. There is always a one deep delay when writing the CFG register. Note that, at power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions. Thus CFG [13:0] = 0x3FFF. This sets the ZJC2102-14 for the following:

- IN [7:0] unipolar referenced to GND, sequenced in order
- Full bandwidth
- Internal reference and temperature sensor disabled, buffer enabled
- Internal sequencer enabled
- No readback of the CFG register

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC	INCC	INCC	INX	INX	INX	BW	REF	REF	REF	SEQ	SEQ	RB

Configuration Register Description:

<table>
<tr><th>Bit</th><th>Name</th><th colspan="4">Description</th></tr>
<tr><td>[13]</td><td>CFG</td><td colspan="4">Configuration update.
0 = write invalid, keep current configuration settings.
1 = write enabled, overwrite contents of register.</td></tr>
<tr><td rowspan="8">[12:10]</td><td rowspan="8">INCC</td><td colspan="4">Input channel configuration. Selection of pseudo differential bipolar, pseudo differential unipolar pairs, single-ended, or temperature sensor.</td></tr>
<tr><td>12</td><td>11</td><td>10</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>X[1]</td><td>Pseudo differential bipolar pairs; INx- input is $V_{REF}/2 \pm 0.1$ V.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Pseudo differential bipolar pairs; INx- is COM = $V_{REF}/2 \pm 0.1$ V.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Temperature sensor.</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>Pseudo differential unipolar pairs; INx- input is GND ± 0.1 V.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Pseudo differential unipolar pairs; INx- is COM = GND ± 0.1 V.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Singled-ended; INx referenced to GND.</td></tr>
<tr><td rowspan="6">[9 :7]</td><td rowspan="6">INx</td><td colspan="4">Input channel selection.</td></tr>
<tr><td>9</td><td>8</td><td>7</td><td>Channel selected.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>IN0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IN1</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN7</td></tr>
<tr><td>[6]</td><td>BW</td><td colspan="4">Selection of bandwidth for low-pass filter.
0 = ¼ BW, an additional internal series resistor to limit the noise. Maximum throughput must be reduced to ¼.
1 = Full bandwidth.</td></tr>
<tr><td rowspan="5">[5 : 3]</td><td rowspan="5">REF</td><td colspan="4">Reference or buffer selection. Selection of internal, external, external buffered, and enabling of the on-chip temperature sensor.</td></tr>
<tr><td>5</td><td>4</td><td>3</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal reference and temperature sensor enabled. REF = 2.5 V buffered output.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal reference and temperature sensor enabled. REF = 4.096 V buffered output.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Use external reference on REF. Temperature sensor enabled. Internal</td></tr>
</table>

[1] X = do not care

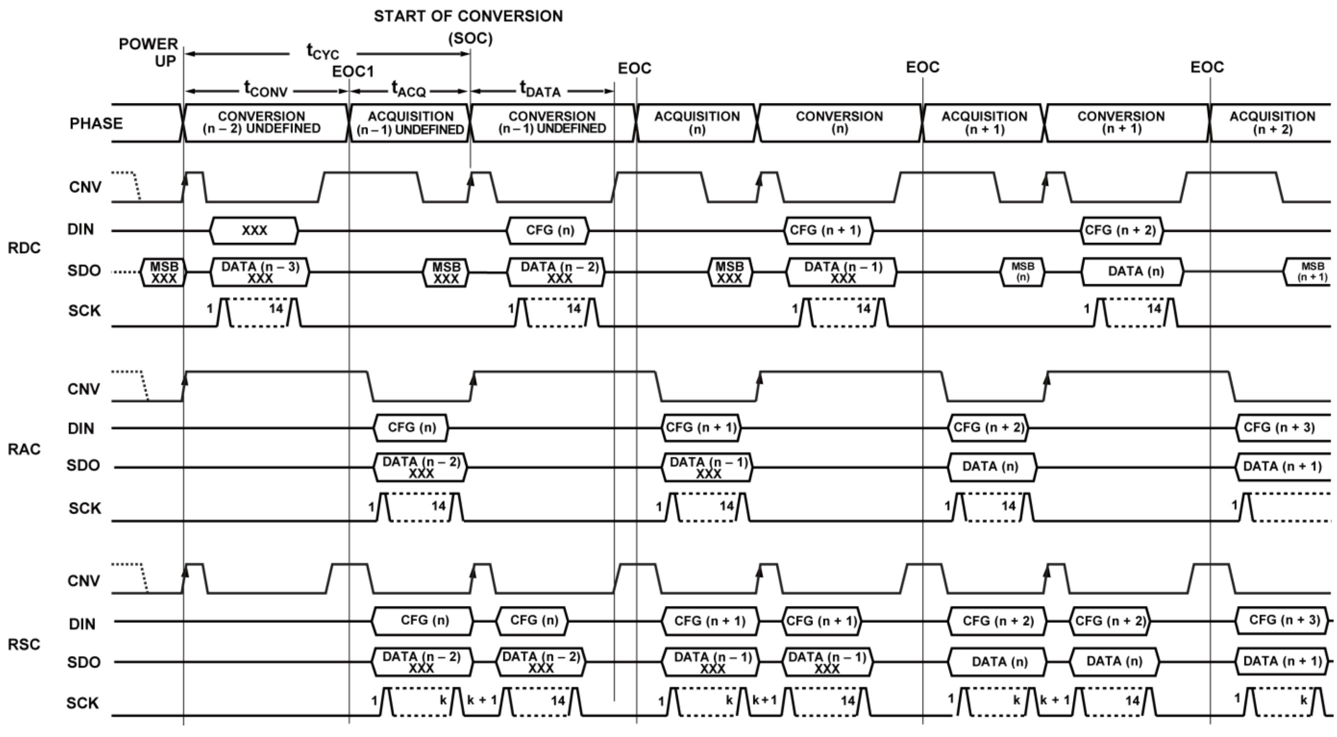
					buffer disabled.
		0	1	1	Use external reference on REFIN. Temperature sensor enabled. Internal buffer enabled.
		1	0	0	Invalid.
		1	0	1	Invalid.
		1	1	0	Use external reference on REF. Temperature sensor disable, internal reference disabled and internal buffer disabled.
		1	1	1	Use external reference on REFIN. Temperature sensor disable, internal reference disabled and internal buffer enabled.
[2 : 1]	SEQ	Channel sequencer. Allows for scanning channels in an IN0 to IN [7:0] fashion.			
		2	1	Function	
		0	0	Disable sequencer.	
		0	1	No effect.	
		1	0	Scan IN0 to IN [7:0] (set in CFG [9:7]), then temperature.	
		1	1	Scan IN0 to IN [7:0] (set in CFG [9:7])	
[0]	RB	Read back the CFG register. 0 = Read back current configuration at end of code. 1 = Do not read back current configuration at end of code.			

General Timing Without a Busy Indicator

Figure 39 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). Note that the gating item for both CFG and code readback is at the end of conversion (EOC). Make sure CNV is high at EOC, so the busy indicator is disabled.

The data access should happen during the safe data reading/writing time, t_{DATA}. If the full CFG word was not written to before EOC, it is discarded and the current configuration remains. If the conversion result is not read out fully prior to EOC, it is lost as the ADC updates SDO with the MSB of the current conversion. When CNV is brought low after EOC, SDO is driven from high impedance to the MSB. Falling SCK edges clock out bits starting with MSB −1. The SCK can idle high or low.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the 2nd EOC; thus two dummy conversions are required. Also, if the state machine writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. Note that the first valid data occurs in Phase (n + 1) when the CFG register is written during Phase (n - 1).



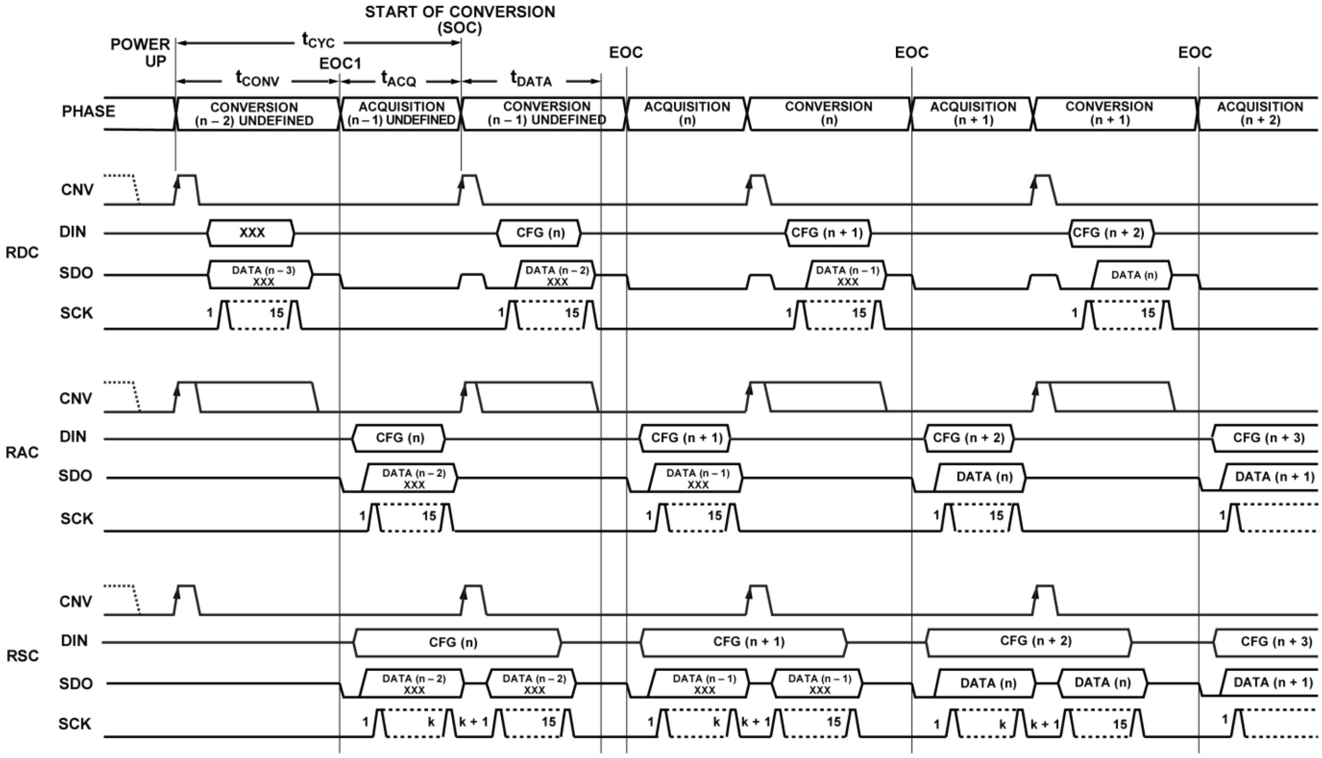
Note: n =14 for no readback of CFG; n = 28 for readback of CFG

Figure 39. General Interface Timing for the ZJC2102-14 Without a Busy Indicator

General Timing with a Busy Indicator

Figure 40 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). If CNV is low at EOC, the busy indicator is enabled. In addition, to generate the busy indicator properly, the host must provide a minimum of 15 SCK falling edges to return SDO to high impedance because the last bit on SDO remains active.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the 2nd EOC; thus two dummy conversions are required. If the host writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. Note that the first valid data occurs in Phase (n + 1) when the CFG register is written during Phase (n - 1).



Note: n = 15 for no readback of CFG; n = 29 for readback of CFG

Figure 40. General Interface Timing for the ZJC2102-14 With a Busy Indicator

Channel Sequencer

ZJC2102-14 channels can be scanned as singles or pairs, with or without the temperature sensor.

The sequencer starts with IN0 and ends with IN [7:0] set in CFG [9:7]. For paired channels, the channels are paired depending on the last channel set in CFG [9:7]. Note that in sequencer mode, the channels are always paired with the positive input on the even channels (IN0, IN2, IN4, IN6), and with the negative input on the odd channels (IN1, IN3, IN5, IN7).

Figure 41shows the timing for all three modes without a busy indicator. The sequencer can also be used with the busy indicator.

For sequencer operation, the CFG register should be set during the (n - 1) phase. On phase (n), the sequencer setting takes place and acquires IN0. The first valid conversion code is available at phase (n + 1). After the last channel set in CFG [9:7] is converted, the internal temperature sensor data is output (if enabled), followed by acquisition of IN0.

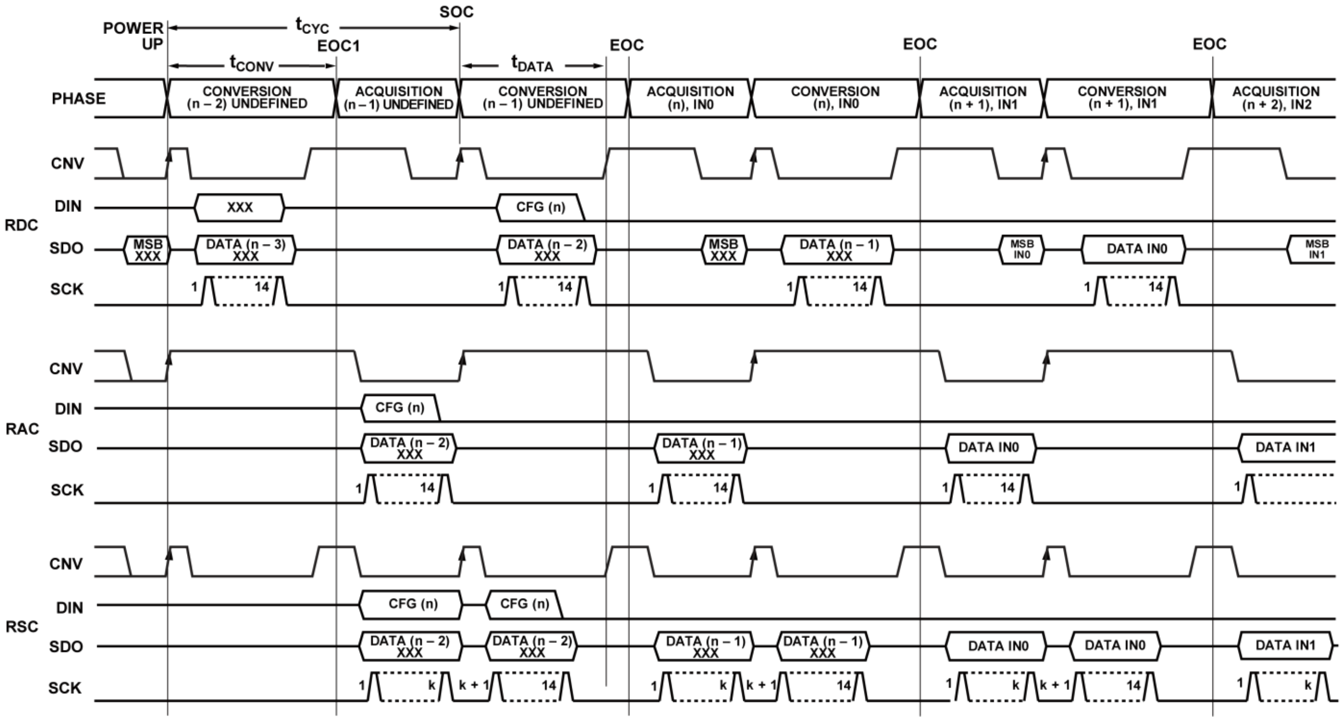


Figure 41. General Channel Sequencer Timing Without a Busy Indicator

RAC Without a Busy Indicator

ZJC2102-14connects to the host as shown in Figure 42, and the timing is shown is Figure 43.

A rising edge on CNV initiates a conversion, pushes SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion independent of the state of CNV. CNV must be returned high before the t_{DATA} elapses, and then held high beyond the conversion time t_{CONV}, to avoid the busy indicator generation.

After the conversion is complete, the ZJC2102-14 enters the acquisition phase and powers down. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 13 SCK falling edges clock out the conversion results starting with MSB - 1. All 14 bits of CFG [13:0] must be written, otherwise they are ignored.

After the 14th (or 28th) SCK falling edge, or when CNV goes high (whichever happens first), SDO returns to high impedance.

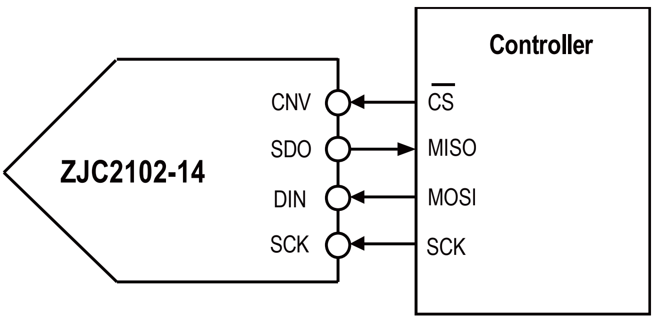


Figure 42. Connection without a Busy Indicator

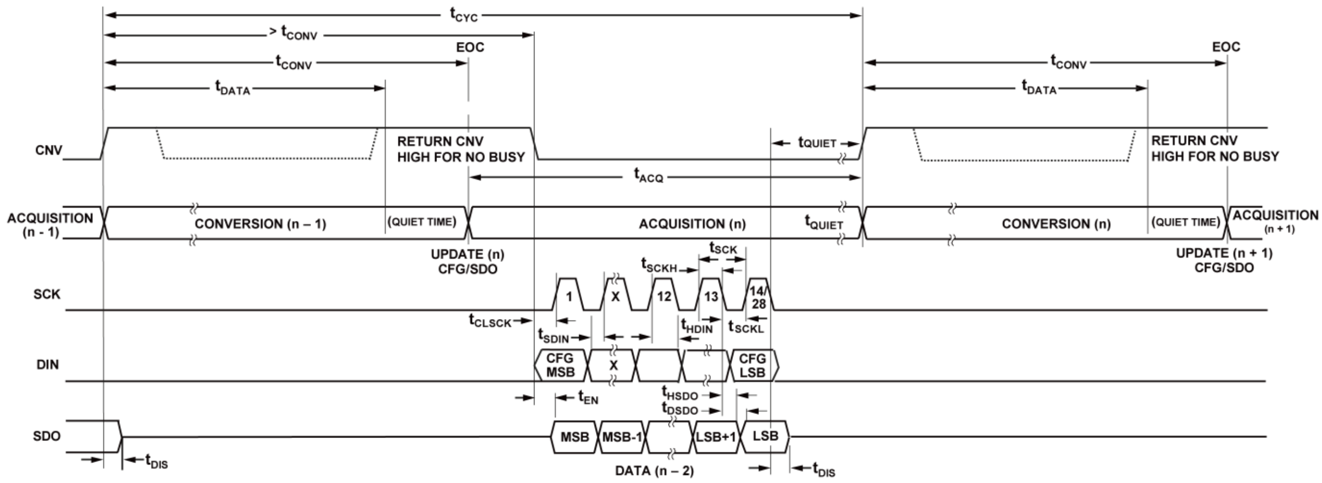


Figure 43. Timing of RAC without a Busy Indicator

RAC with a Busy Indicator

ZJC2102-14 connects to the host as shown in Figure 44, and the timing is shown is Figure 45.

A rising edge on CNV initiates a conversion, pushes SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion independent of the state of CNV. CNV must be returned low before the t_{DATA} elapses, and then held low beyond the conversion time t_{CONV}, to generate the busy indicator.

After the conversion is complete, the ZJC2102-14 enters the acquisition phase and powers down. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 14 SCK falling edges clock out the conversion results. All 14 bits of CFG [13:0] must be written, otherwise they are ignored.

After the 15th (or 29th) SCK falling edge, or when CNV goes high (whichever happens first), SDO returns to high impedance.

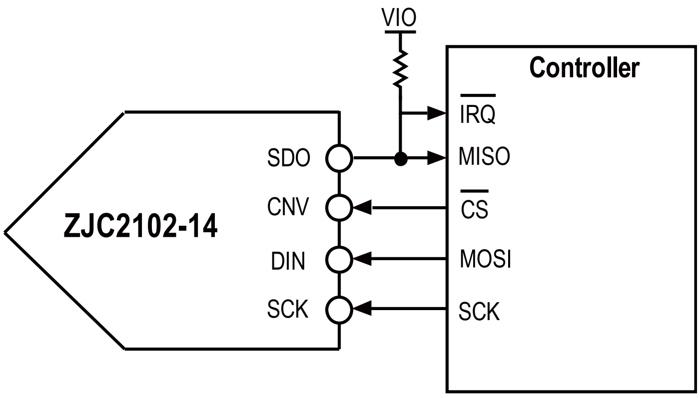


Figure 44. Connection with a Busy Indicator

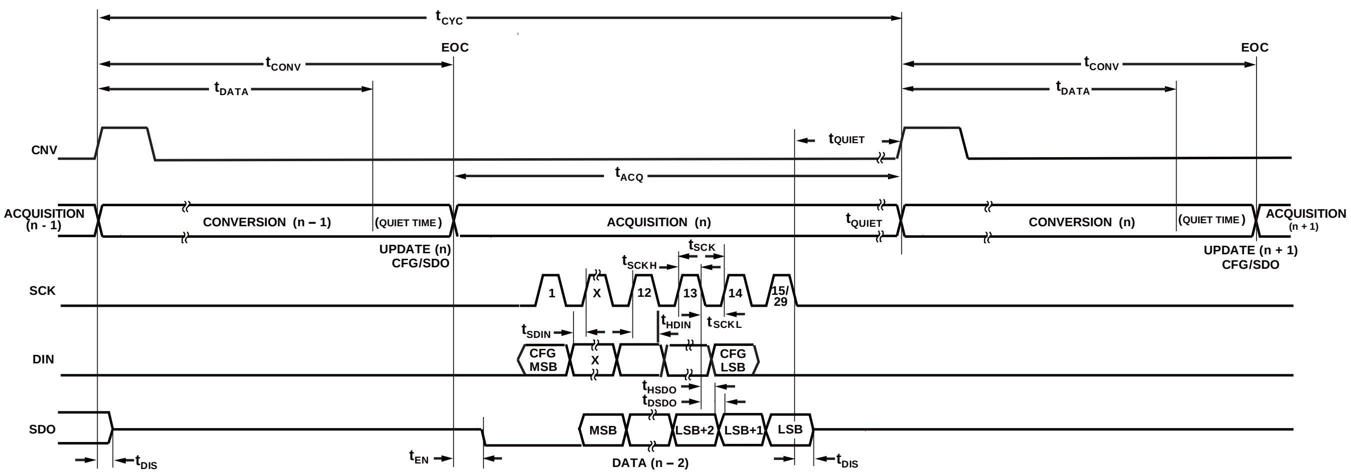


Figure 45. Timing of RAC with a Busy Indicator

Layout Guidelines

For optimum performance of the device, good PCB layout practices are recommended, including:

- Avoid running digital lines under the device, which may couple noise onto the die, unless a ground plane under the ZJC2102-14 is used as a shield. Fast switching signals such as CNV or clocks should not be placed close to the analog signal path. Crossover of digital and analog signals should be avoided.
- At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined close to the ZJC2102-14.
- The ZJC2102-14 external voltage reference input, REF, has a dynamic input impedance and should be decoupled with 10μFceramic capacitors to minimize parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance trace.
- The power supply V_{DD} of ZJC2102-14should be decoupled with 10 μF and 100 nF ceramic capacitors, placed close to the ZJC2102-14 and connected using short, wide traces to provide low impedance paths and to reduce the effect of noises on the power supply lines.

Figure 46 is an example of the guidance.

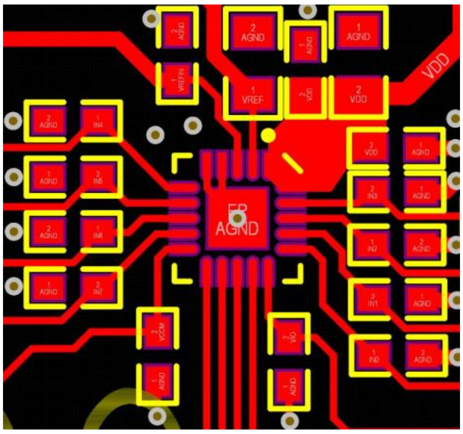


Figure 46.   Example Layout and Routing of ZJC2102-14

Outline Dimensions

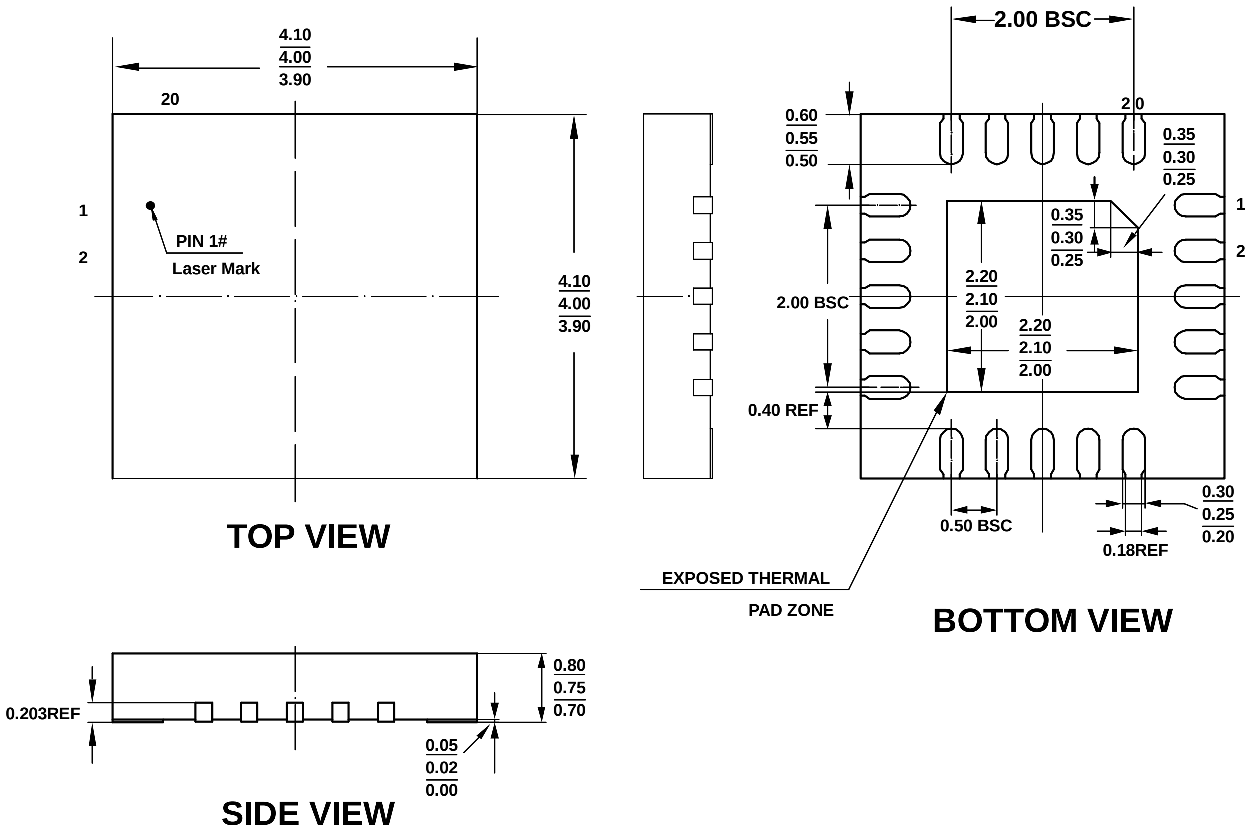


Figure 47. 20-LeadQFN-20 Package Dimensions Shown in Millimeter

Ordering Guide

Model	Package	Orderable Device	Resolution (bit)	Supply Voltage (V)	Temperature Range (°C)	External Package
ZJC2102-14	QFN-20	ZJC2102-14ATPER	14	2.3 to 5.5	- 40 to + 85	13” Reel

Product Order Model

ZJXXXXX X X X X X

- External Package: T = tube; R = reel
- Temperature range: A/B = - 40 °C to 125 °C Automotive/Non - Automotive; E = - 40 °C to 85 °C
- Number of Pins: A = 8; B = 10; D = 14; E = 16; P = 20; T = 6
- Package type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers

Related Parts

Part Number	Description	Comments
ADC		
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8/MSOP-10/DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14/TSSOP-16/QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2/4	Dual/Quad 36 V 7 MHz precision JFET Op Amps	7 MHz GBW, 35 V/µS SR, 50 µV max Vos, 1 µV/°C max Vos drift, 2 mA/Amplifier, RRO, 4.5 V to 35 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ibias, 25 µV max Vosi, gain error 0.001 % max (G = 1), 625 kHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V, - 40 °C to 125 °C specified
ZJA3622/8	36 V low cost precision in-amp	CMRR 93 dB min (G = 10), 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V, - 40 °C to 125 °C specified
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min, Vos 100 µV max, gain error 15 ppm max, 500 kHz BW, 330µA, 2.7 to 36 V
Voltage Reference		
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ±0.05 % initial error
ZJR1001 ZJR1002 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ±0.05 % initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ± 50 V power on & off, latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS, 10 V to 36 V